IMAGE SIGNAL PROCESSING PIPELINE SOLUTION

OVERVIEW

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Helion ENGINEERING VISION

IONOS-IMAGING IP-CORES

Introduction

Helion's experience in image processing enables desginers of embedded vision, video surveillance, automotive and medical imaging systems to use pre-engineered high quality ISP IP cores on their camera systems.

The IONOS ISP IP Cores can be used for pre- and post-processing, image sensor control, FPGA algorithm and DSP algorithm.

Helion offers a comprehensive selection of preconfigured video pipelines, ranging from basic to advanced monochrome and color pipelines, all the way through high resolution, advanced High Dynamic Range Imaging (HDRI) color pipelines.

LATTICE SEMICONDUCTOR

Features

- Supports image sensors up to 16MP resolution
  - Offers seamless upgrade path, protects investment
  - Direct sensor interfaces and setup
- 1080p60 streaming data path through FPGA
  - Supports 1080p at 60 frames per second
  - No external frame buffer required
  - Offers quality at lower system cost
  - Extremely Low latency
- IP supports up to 192 dB (32Bit) scene dynamic range
  - Maximum details under difficult lighting conditions
  - Exceeds the 150dB automotive manufacturer
  - HDRI Tonemapping available
  - Hybrid log Mode support
- Wishbone compatible IP and Mico32 support
  - Easy to setup and use
  - Double-click interconnect solution
  - Platform library and structure header files
- Comprehensive IP Suite
  - End to end ISP solutions
- ISPs are Optimized for Lattice's ECP3™ and ECP5™ architecture
- IPs are available for Crosslink™, XO3™, XP2™, ECP2™, ECP3™, ECP5™

Helion is an IP Core partner of Lattice for many years now. Helion has teamed up with Lattice to deliver software reference designs for several development kits, like HDR60 or the new Embedded Vision Development Kit.

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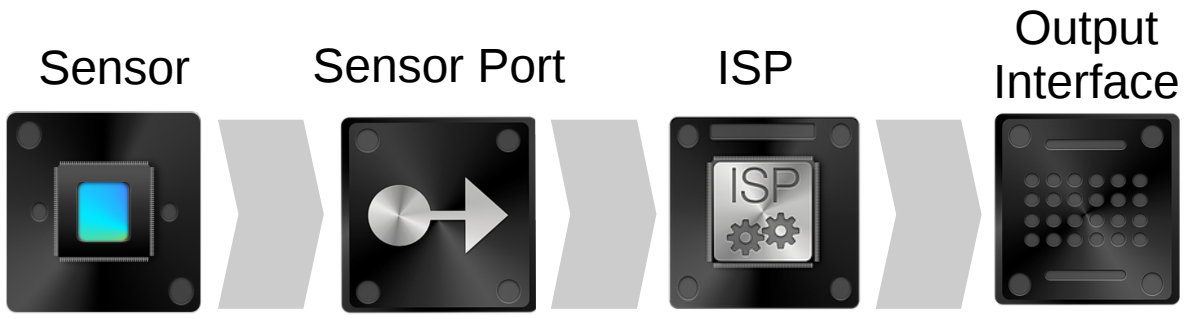
Fast Time to Market with IONOS ISP

Helion offers a comprehensive selection of image processing pipelines, ranging from basic to advanced high dynamic range ISPs, which can be quickly evaluated on the Lattice embedded vision camera development kit.

Containing a library of more than 100 individual IP Cores for licensing either entirely or in parts.

ISP Blockdiagram



Overview of ISP Solutions

Standard HD ISP

- 12Bit 12 Bit per Color
- DPC Defect Pixel Correction
- CFI Color Filter Interpolation
- CCM Color Correction Matrix
- CSM Color Saturation Matrix
- AWB Automatic White Balance
- Y Gamma Correction
- TP Test Pattern Generator
- STAT Statistic
- CI Config Interface

Enhanced HD ISP

All features Standard HD ISP

- 16Bit 16 Bit per Color
- LSC Lens Shading Correction
- GCM Green Channel Mismatch
- AC Aperture Correction
- NR 2D Noise Reduction
- IE Image Enhancer
- HS Histogram Statistics
- HDR High Dynamic Range

Enhanced DR HD ISP

All features Enhanced HD ISP

- 32Bit 32 Bit per Color

*Bypass function for every IP Core possible
*RAW Bypass possible (all modules at once)

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IONOS-IMAGING IP-CORES

Part of the most used IP in ISPs

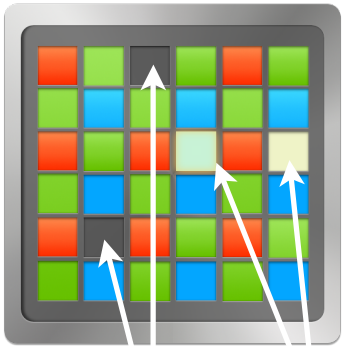
DPC- Defective Pixel Correction

Functional Description

Defective cold or hot pixels, are corrected with the defective pixel correction IP core. This corrects the defective pixel with interpolated values based on neighbor pixels of the same color channel.

Typical correction methods include detection of cold or hot pixels using either median or averaging estimation on immediate pixel neighborhood.

Bayer-Pixel Array

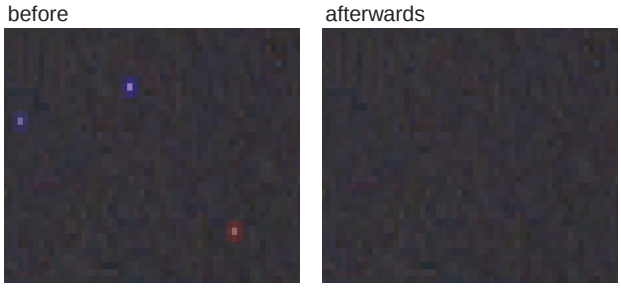


Defective Cold Pixel

Defective Hot Pixel

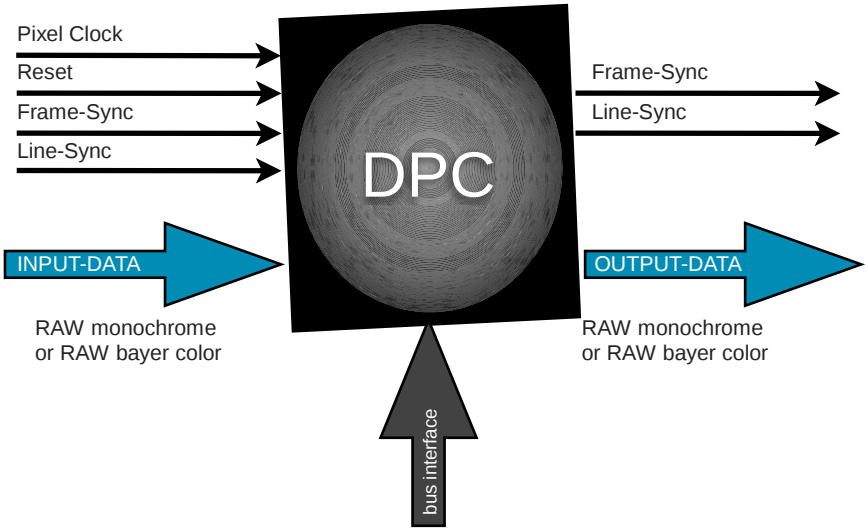
Features

- Selectable bit-width (1..32Bit) for input pixel data
- Image resolution up to 16MP
- Support 1k, 2k, 4k and 8k resolution
- RAW monochrome (3x3) or RAW Bayer color (5x5) filter array
- Median or mean value filter version available
- Maintaining of sync signal timing
- Low latency (4 lines)
- Stream operation
- Dynamic setup with bus interface
  - Extrapolation or skipping of picture border pixels
  - Switch off complete module (bypass function)



Included in ISP

- Standard HD ISP
- Enhanced HD ISP
- Enhanced Dynamic Range HD ISP
- ECO HD ISP
- UHDTV



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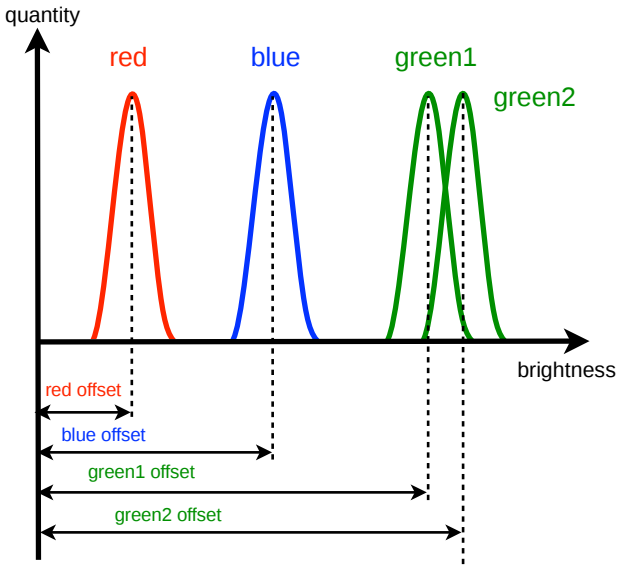
BLC- Black Level Correction

Functional Description

Each color channel has a time dependent offset. Color processing requires linear signal behaviors. Therefore all signals must be without any offset. Every CMOS sensor has light insesitive cells next to the active image area, called dark rows.

This IP core utilizes subtraction of the color channel-specific, dark level offsets, to achieve an optimal black level result.

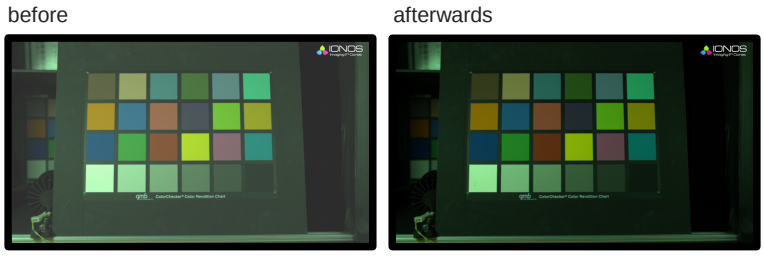
Color Offset



Features

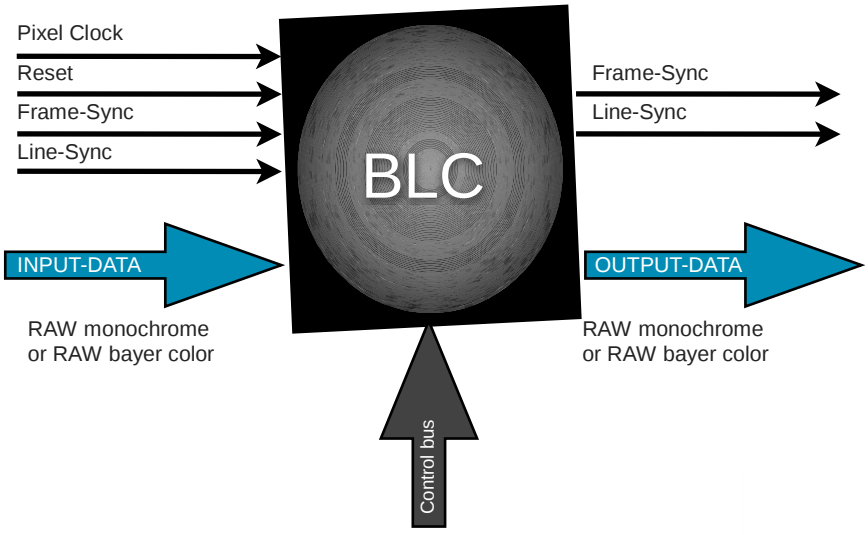
- Selectable bit-width (1..32Bit) for input pixel data
- Image resolution up to 16MP
- Support 1k, 2k, 4k and 8k resolution
- HD ready (720p/1080p)
- Each color channel processed separately

- Dynamic Setup via bus interface
  - Adjustable integration time for black offset
  - Identification
  - Selectable position of dark rows/columns
  - Switch off complete module (bypass function)



Included in ISP

- Standard HD ISP
- Enhanced HD ISP
- Enhanced Dynamic Range HD ISP
- ECO HD ISP
- UHDTV



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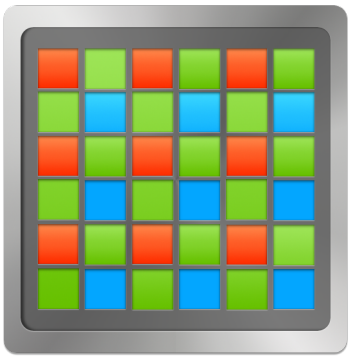
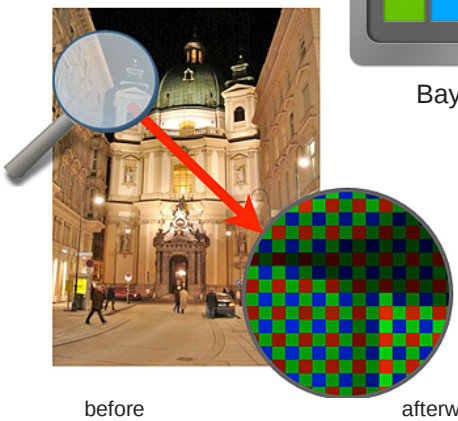
CFI- Color Filter Interpolation (Debayering)

Functional Description

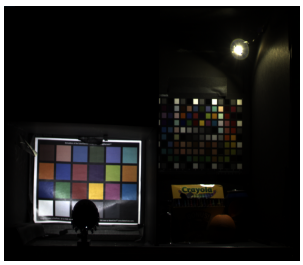
Each sensor pixel has a filter with one of three colors (R/G/B), this results that two-thirds of the color data is missing in a pixel. Reconstruction of the original image requires the use of demosaicing algorithms which are required to interpolate a set of red, green, and blue values for each pixel.



Bayer-Pixel Array



before



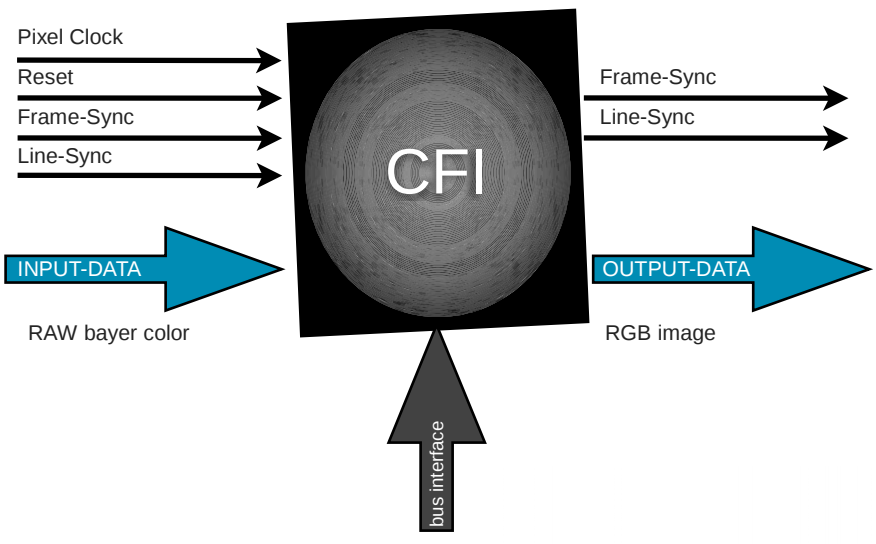
afterwards

Features

- Selectable bit-depth (1..32Bit) for input pixel data
- Image resolution more than 16MP
- Support 1k, 2k, 4k and 8k resolution
- Arbitrary picture size
- Reset input
- Short latency (4 lines)
- Different algorithms available
  - 3x3 bilinear
  - 5x5 high-quality or
  - 3x3 debayer with edge detection
- Dynamic setup with bus interface
  - Border extrapolation
  - Definition of first bayer phase
  - Switch off complete module (bypass function)

Included in ISP

- Standard HD ISP
- Enhanced HD ISP
- Enhanced Dynamic Range HD ISP
- ECO HD ISP
- UHDTV



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Part of the most used IP in ISPs

CCM- Color Correction Matrix

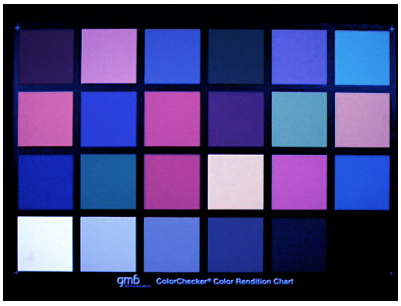
Functional Description

Image acquisition is the most important process in high quality image processing. However, a variety of image sensors possess incorrect color rendition due to so called cross-color effects. This effects leads to wrong color images (e.g. green with too much blue). The IONOS CCM IP-core will correct this behavior.

Adjustment of each single color channel by a 3x3 correction matrix.

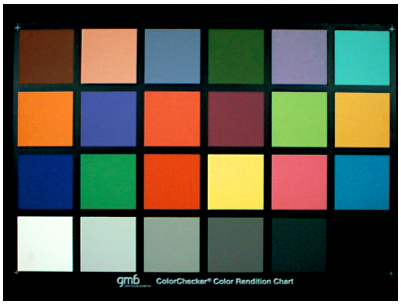
red-out	=rr*red+rg*green+rb*blue
green-out	=gr*red+gg*green+gb*blue
blue-out	=br*red+bg*green+bb*blue

original sensor data



D65

CCM



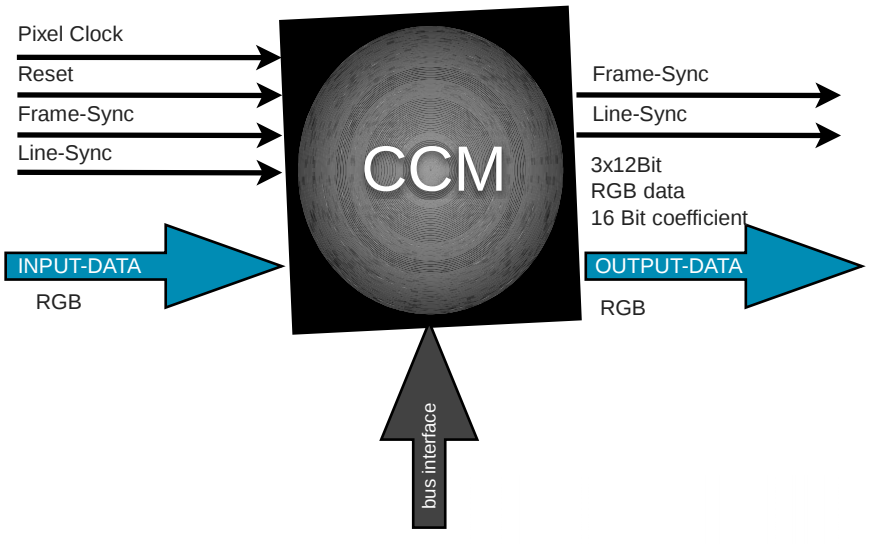
D65

Features

- Selectable bit-depth
  (1..32Bit) for input pixel data, HDR/WDR ready
- Image resolution up to 16MP
- Support 1k, 2k, 4k and 8k resolution
- 18 Bit coefficient with fixed point value
- RGB in- and output
- Auto saturation detection
- Dynamic setup with bus interface
  - Each matrix coefficient can be moditied through runtime
  - Switch off complete module (bypass function)

Included in ISP

- Standard HD ISP
- Enhanced HD ISP
- Enhanced Dynamic Range HD ISP
- ECO HD ISP
- UHDTV



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γ - Gamma Correction

Functional Description

Pixels are illuminated in a linear way. To provide pixel data to common video systems a conversion to a non-linear value encoding may be needed.

Gamma correction provides conversion of a RGB-input signal from linear to non-linear value and vice versa. This function uses arbitrary gamma correction factors.

γ=1.0

CCM

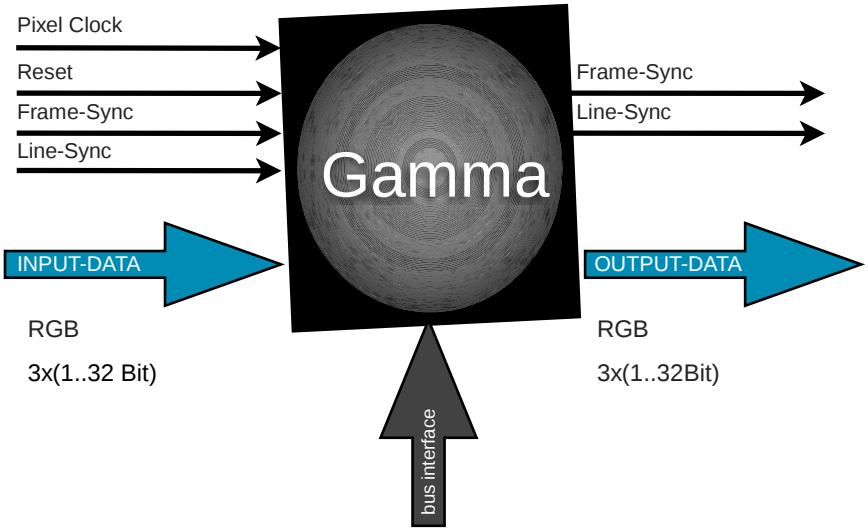
γ=0.5

Features

- Selectable bit-depth (1..32Bit) for input pixel data
- Image resolution up to 16MP
- Support 1k, 2k, 4k and 8k resolution
- Selectable output data-width (for RGB)
- For all colors, one look up table which is mapped into the memory address space
- Single reset-input for global / local reset
- Separate correction for each color channel
- Dynamic Setup via bus interface
  - flexible modification of table entries
  - Switch off complete module (bypass function)

Included in ISP

- Standard HD ISP
- Enhanced HD ISP
- Enhanced Dynamic Range HD ISP
- ECO HD ISP
- UHDTV



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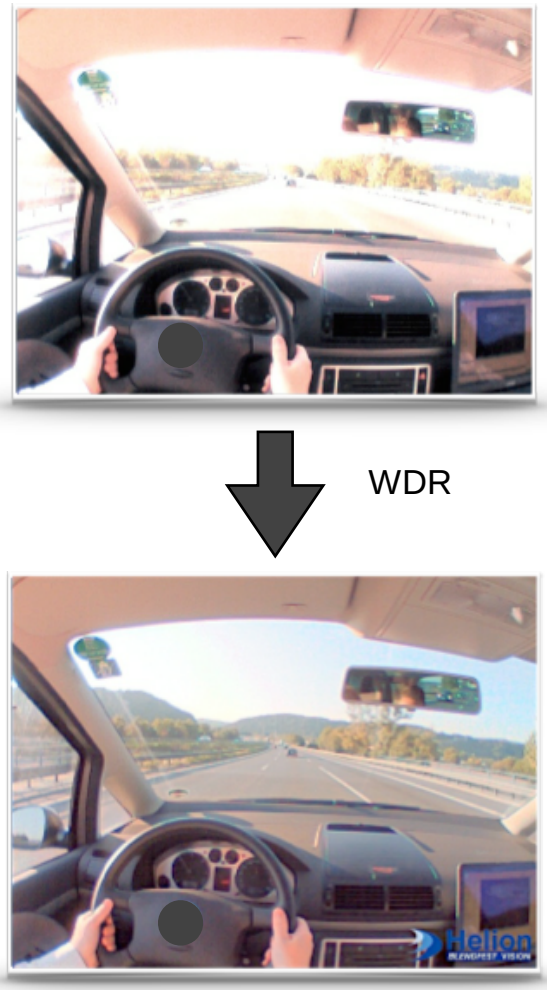
Part of the most used IP in ISPs

WDR – Wide Dynamic Range Tone-mapping

Functional Description

Fully configurable comprehensive High Dynamic Range (HDR) IP-core, which works with industry standard HDR sensors, and delivers outstanding HDR performance.

Extremely wide 120dB-HDR-IP core ensures that no detail in dark areas is lost even when an light source shines directly into the camera lens. While HDR is working in close conjunction with a fast-Auto-exposure it rapidly adjusts exposure in changing light conditions to offer a system dynamic range of 170dB (sensor dependent).

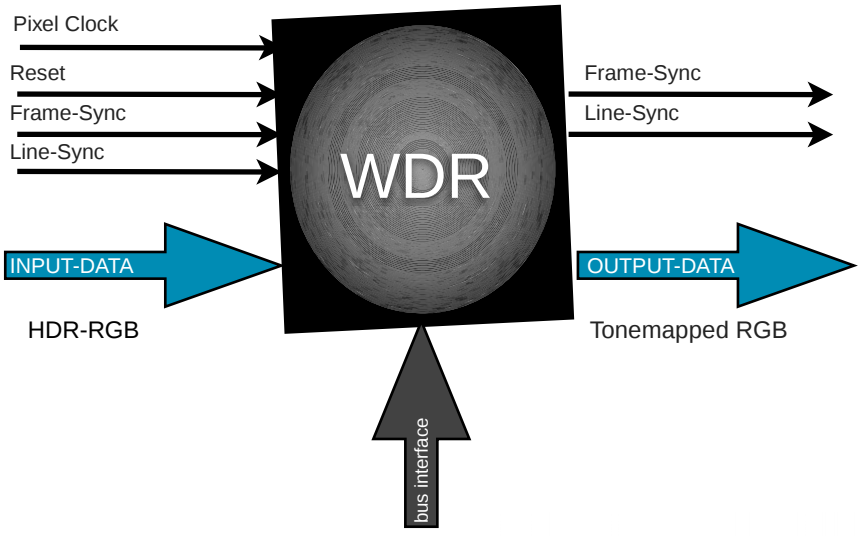


Features

- Selectable bit-depth (1..32 Bit) for each RGB color channel
- Selectable output bit-depth
- Image resolution up to 16MP
- Support 1k, 2k, 4k and 8k resolution
- No external memory needed
- Brightness dependent tone-mapping
- Dynamic setup with bus interface
  - Fully configurable transfer curve
  - Linear mapped memory address space
  - Switch off complete module (bypass function)
  - Support of Hybrid log mode

Included in ISP

- Enhanced HD ISP
- Enhanced Dynamic Range HD ISP
- UHDTV



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IP library Overview

ISP: Image Signal Processing
IE: Image Enhance
GEN: Generic
OVL: Overlay
SP: Sensor Port
OUT: Output Interface

Pos.	IP- Cores	IP- Class	ECO HD ISP (9 Bit)	Standard HD ISP (12 Bit)	Enhanced HD- ISP (16 Bit)	Enhanced DR HD ISP (32 Bit)
1	CFI, Color Interpolation, 3x3 Bilinear Debayer	ISP				
2	CFI, Color Interpolation, 3x3 Smart Debayer	ISP	x			
3	CFI, Color Interpolation, 5x5 HQ Debayer	ISP		x	x	x
4	Color Interpolation, double 3x3 HQ Debayer	ISP				
5	CCM Color Correction Matrix	ISP	x	x	x	x
6	CCM Color Saturation Matrix	ISP		x	x	x
7	Luminance Adaptive Color Desaturation	ISP				
8	Gamma Correction	ISP	x	x		
9	Gamma Correction with linear interpolation	ISP			x	x
10	Mono gain, 16.16 Bit fixed point gain	ISP	x	x	x	x
11	RGB gain, 16.16 Bit fixed point gain	ISP	x	x	x	x
12	2 channel mixer with 256 mixing stages	ISP				
13	Pixel Clock Detector	ISP				
14	Green-Channel Balancing	ISP			x	x
15	AWB Automatic White Balance	ISP	x	x	x	x
16	3D Noise Reduction (external RAM needed)	IE				
17	2D Noise Median Filter	IE			x	x
18	DPC, 2D Defect Correction on the Fly	ISP		x	x	x
19	DPC, 1D Defect Correction on the Fly	ISP	x			
20	Lensshading Correction (one channel, e.g. Luminance)	ISP				
21	Lensshading Correction (three channel, e.g. RGB)	ISP			x	x
22	Generic Filter Kernel with 3x3 user matrix	GEN				
23	Delay line	GEN				
24	3x3 delay line core	GEN				
25	5x5 delay line core	GEN				
26	Full pipelined divider	GEN				
27	Aperture Filter with selectable Strength	IE			x	x
28	Sobel Filter	IE				
29	Global Motion Vector Estimation	GEN				
30	AE Fast Auto Exposure, LDR-Fast-AE	SP				
31	AE Iterative Linear Auto Exposure, LDR-AE	SP				
32	AE High Dynamic Range Fast Auto Exposure HDR-Fast-AE	SP				
33	AE Antiflicker Option for LDR-AE and HDR-AE	SP				
34	Sensor specific AE for MT9M024 in HDR mode	SP				
35	Sensor specific AE for MT9M024 in linear mode	SP				
36	Sensor specific AE for AR0331 in HDR mode	SP				
37	Sensor specific AE for AR0331 in linear mode	SP				
38	Sensor specific AE for MN34041 in linear mode	SP				
39	Sensor specific AE for IMX104/136/236 in HDR mode	SP				
40	Sensor specific AE for IMX104/136/236 in linear mode	SP				
41	Sensor specific AE for VITA1300 in linear global-shutter mode	SP				
42	BLENDFEST HDRI V1 (gain based) monochrom (up to 32 bit)	ISP				
43	BLENDFEST HDRI V1 (gain based) color (up to 32 bit per color channel)	ISP				
44	BLENDFEST HDRI V2 (ratio based) monochrom (up to 32 bit)	ISP				
45	BLENDFEST HDRI V2 (ratio based) color (up to 32 bit per color channel)	ISP			x	x
46	Framerate Converter (30fps->60fps + ext. SRAM)	OUT				
47	Color Space Conversion with downsampling (24 Bit RGB (4:4:4) -> 16 Bit YCr YCb (4:2:2))	OUT				
48	Color Space Conversion with upsampling (16 Bit YCr YCb (4:2:2) -> 24 Bit RGB (4:4:4)	OUT				
49	Color Space Conversion (24 Bit RGB (4:4:4) -> 24 Bit YCrCb(4:4:4)	OUT				
50	Color Space Conversion (24 Bit YCrCb (4:4:4) -> 24 Bit RGB (4:4:4)	OUT				
51	Color Space Conversion with downsampling (Bit RGB (4:4:4) ->YUV420P (4:2:0)) + ext. RAM	OUT				
52	Color Space Conversion witgh upsampling (YUV420P (4:2:0) -> RGB (4:4:4)) + ext. RAM	OUT				
53	Error Diffusion Dithering 1-Way	OUT				
54	Error Diffusion Dithering 2-Way	OUT				
55	OSD On Screen Display Character Map (OSD-CM) 2048 Characters Character/Symbol Generator (OSD-CG)	OVL				
56	OSD Overlay Bitmap 1024x512 with 4x 32 Bit ARGB colors	OVL				
57	OSD Overlay Bitmap 512x256 with 4x 32 Bit ARGB colors	OVL				
58	OSD Overlay Bitmap 128x64 with 4x 32 Bit ARGB colors	OVL				
59	Overlay with one graphical object selectable color, transparency and dimension (16384 Pixel)	OVL				

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IP library Overview

ISP: Image Signal Processing
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GEN: Generic
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SP: Sensor Port
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Pos.	List of IP- Blocks	IP Class	ECO HD ISP (9 Bit)	Standard HD ISP (12 Bit)	Enhanced HD- ISP (16 Bit)	Enhanced DR HD ISP (32 Bit)
60	Rotate (+ ext. SRAM)	IE				
61	Polyphase Scaler (third party)	IE				
62	Keystone Correction	IE				
63	JPG Encoder, full Pixelclock (third party)	OUT				
64	Output Interface with FIFO for µC or DSP	OUT				
65	Output Interface for TFT-Panel	OUT				
66	Output Interface for DVI Transmitter	OUT				
67	Output Interface with BT656-Syncs for video encoder	OUT				
68	Output Interface with BT1120-Syncs	OUT				
69	APIX TX Interface with Setup ROM	GEN				
70	APIX RX Interface with Setup ROM	GEN				
71	Image Sensor Setup and Capture	SP				
72	Parameter Inserting (selectable)	GEN				
73	I2C Fast Framewise Configurator	SP				
74	I2C Slave with 1024 Byte Registermap	GEN	x	x	x	x
75	Testpattern Generator	GEN		x	x	x
76	Terminal style UART configuration	GEN				
77	Simple DMA controller with one additional Wishbone	GEN				
78	Accumulative DMA controller with one additional Wishbone	GEN				
79	LUT DMA controller with one additional Wishbone	GEN				
80	Port Watcher, DMA based	GEN				
81	ID Register	GEN	x	x	x	x
82	System clock counter 64 Bit	GEN				
83	Helion micro code sequencer	GEN				
84	PWM output	GEN				
85	Wishbone Memoryblock with external access port	GEN	x	x	x	x
86	Wishbone LUT with external access port and linear interpolation	GEN				
87	Wishbone Slave Quadoutport 4x 32 Bit	GEN				
88	Wishbone Slave Quadoutport 4x 32 Bit with extra port clock	GEN	x	x	x	x
89	Wishbone Slave Quadinport 4x 32 Bit	GEN	x	x	x	x
90	Wishbone Slave Singleoutport 32 Bit	GEN				
91	Wishbone Slave Singleoutport 32 Bit with extra port clock	GEN				
92	Wishbone Slave Singeinport 32 Bit	GEN				
93	Wishbone Slave Octaoutport 8x 32 Bit	GEN				
94	Wishbone Slave Octaoutport 8x 32 Bit with extra port clock	GEN				
95	Wishbone Slave Octainport 8x 32 Bit	GEN				
96	Wishbone Slave Hexaoutport 16x 32 Bit	GEN				
97	Wishbone Slave Hexaoutport 16x 32 Bit with extra port clock	GEN				
98	Wishbone Slave Hexainport 16x 32 Bit	GEN				
99	Wishbone Slave Hexainhexaoutport 2x 16x 32 Bit	GEN				
100	Wishbone Slave Hexainhexaoutport 2x 16x 32 Bit with extra port clock	GEN				
101	Wishbone I2C Master	SP				
102	Wishbone I2C Slave with 256 Registers	GEN	x	x	x	x
103	Image Statistics, mono HDR	ISP				
104	Image Statistic, RGB HDR, 4x4 fields	ISP				
105	Image Statistic, RGB HDR	ISP	x	x	x	x
106	Image Histogram	ISP	x		x	x
107	SDRAM based multi port streaming memory controller	GEN				
108	DDR2 based multi port streaming memory controller	GEN				
109	SRAM based multi port streaming memory controller	GEN				
110	DDR3 based multi port streaming memory controller	GEN				
111	AF Sobel Filter	IE				
112	AF Statistic module	IE				
113	AF Library	IE				

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Pos.	List of IP- Blocks	IP Class	ECO HD ISP (9 Bit)	Standard HD ISP (12 Bit)	Enhanced HD- ISP (16 Bit)	Enhanced DR HD ISP (32 Bit)
114	Sensor Port for MT9M024 in HDR mode	SP				
115	Sensor Port for MT9M024 in linear mode	SP				
116	Sensor Port for AR0331 in HDR mode	SP				
117	Sensor Port for AR0331 in linear mode	SP				
118	Sensor Port for MN34041 in linear mode	SP				
119	Sensor Port for IMX104/136/238/236 in HDR mode	SP				
120	Sensor Port for IMX104/136/238/236 in linear mode	SP				
121	Sensor Port for SONY	SP				
122	Sensor Port for PANASONIC	SP				
123	Sensor Port for CMOSIS	SP				
124	ECO HD-ISP	ISP	x			
125	Standard HD-ISP	ISP		x		
126	Enhanced DR HD-ISP	ISP			x	
127	HDR HD-ISP	ISP				x
128	UHDTV-ISP	ISP				
129	GigEVision	OUT				

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IP-Licensing Options / Evaluation License for Lattice Test Drives

Procedure of SDK Evaluation (SDK = Test Drive) and Sample Source Code

Step 1
Trial (free of charge)

Kit is pre-loaded with demo bitstream
Customer can use the GUI (ICG) to setup AE, AWB, colors, contrast, gamma...

Step 2
In-depth evaluation (free of charge)

Customer has to sign free of charge **IONOS Evaluation License** by Helion.
This License grant access to SW reference designs.

Customer can start first tests and developments on own Hardware, on HDR60 or Embedded Vision Development Kit.

Step 3
Preparation of product development and during development

Customer can buy prepaid support packages by Helion.
Support packages 01: Project Workshops
Support packages 02: Trainings (Sensor, ISP or FPGA)
Support packages 03: Consulting and Development
(Please contact: **sales@helionvision.com** for further information regarding the support packages)

Step 4
If the project is close to finish and if the customer wants to generate bit streams for production the customer has to sign the production license agreement.

Signing the evaluation IP licensing agreement with Helion *

Please send a mail to: sales@helionvision.com
Subject: Evaluation License Embedded Vision - IONOS-ISP

•Evaluation IP licensing:
By signing the evaluation IP licensing agreement with Helion, customers will have access to Helion's complete IP suite at no cost.

The IP suite includes documentation, **time- limited** IP- Cores and ISP pipeline example projects.

• Production IP licensing:
By signing the production IP licensing agreement, customers keys are provided by Lattice to unlock the time limited IP-Cores in the diamond software.

For further license information and the evaluation license agreement please check:

http://www.helion-vision.com/dpc-c1n8i

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