IONOS-ISP Evaluation on Lattice HDR-60
Camera Development Kit

IONOS-IMAGING IP-CORES

ICG - Ionos Configuration GUI Quick Start Guide

Revision 20022014-v1s04

www.helionvision.com

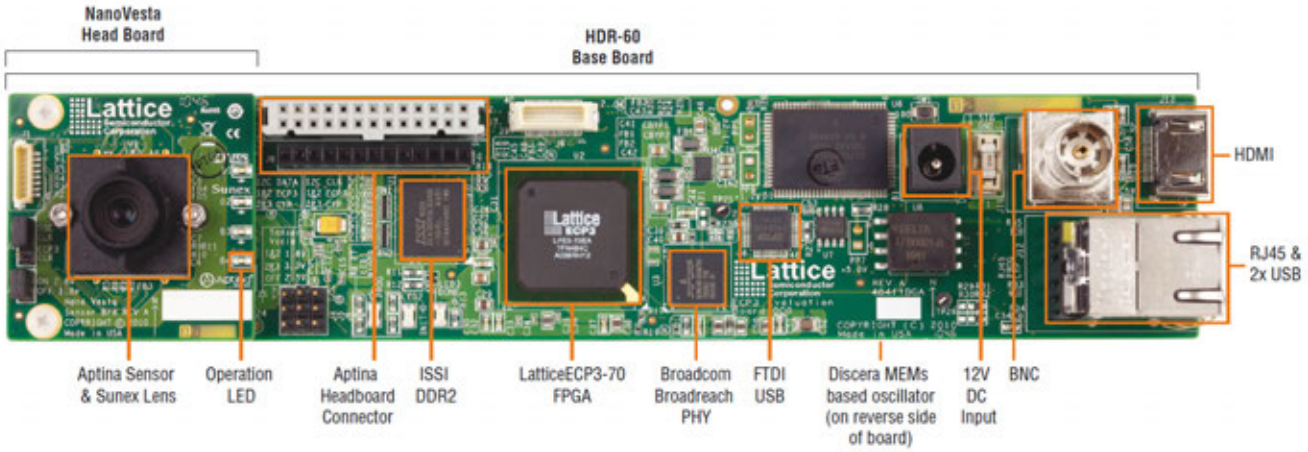
Helion
ENGINEERING VISION

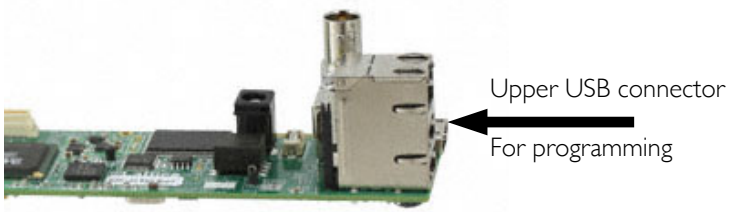
CONTENTS

CHAPTER 1
Kit Content

- HDR-60 Base Board with LatticeECP3™ FPGA, pre-loaded with Image Signal Processing (ISP) Demo
- NanoVesta Head Board with Aptina sensor and Sunex lens (included with-DKN version only)
- Two USB cables
- HDMI cable with HDMI-to-DVI adapter
- 12 V AC adapter power supply
- QuickSTART Guide

Note: Static electricity can shorten the lifespan of electronic components. Please handle the kit components carefully. Mechanical stress can damage the board. Please handle the Board carefully.





This document provides a brief introduction and instructions to install and demonstrate the HDR-60 Video Camera Development Kit on Windows 7/Vista/XP/2000. Additional documentation can be downloaded at www.latticesemi.com/hdr60 . The HDR-60 Base Board User's Guide and NanoVesta Head Board User's Guide are also available for download from the Lattice web site.

Note:
The upper USB connector utilizes the FTDI USB device for programming different designs into the LatticeECP3-70 device. Programming the LatticeECP3 device requires Lattice "Programmer Standalone". The software can be downloaded after a free registration from the Lattice web site at www.latticesemi.com

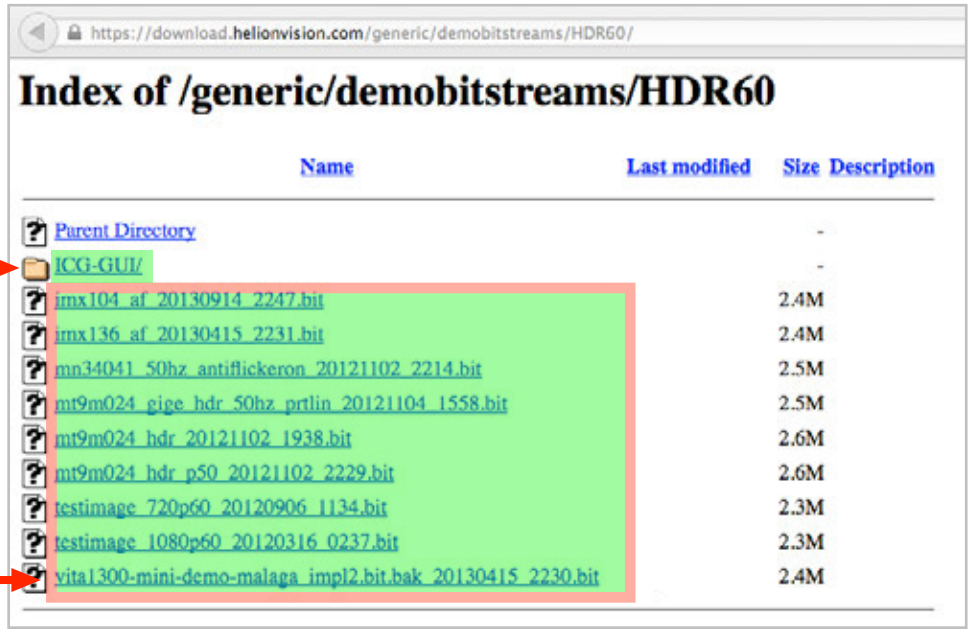
CHAPTER 2
Quick Setup Guide

2.1 Downloading the Helion Bitstreams

Please download the latest ICG version and the suitable bitstream for your board at:
https://download.helionvision.com/generic/demobitstreams/HDR60/

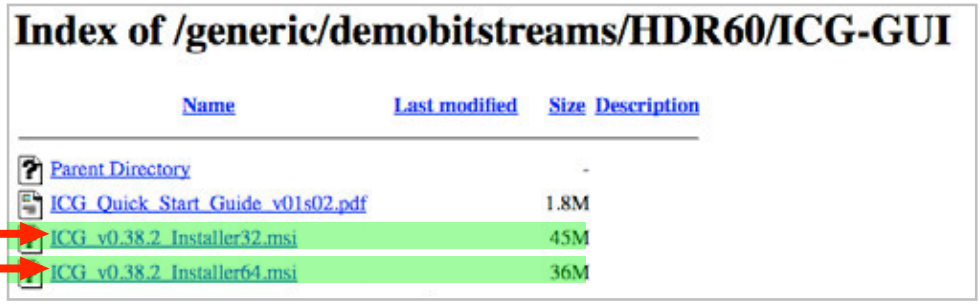
(1) ICG-Folder

(3) Latest ICG version for your Image Sensor



Picture 2.1: Demobitstream-Directory

(2) msi-files for the operating system



Picture 2.2: ICG-GUI-Directory

Click on the ICG-GUI-Folder (1) and choose the right ".msi" (2) file for your operating system (32 or 64 Bit). After, you can choose in the Demobitstream-Directory the right ".bit" (3) file for your image sensor and download it.

Note: You will need this bitstream later. See also page 7

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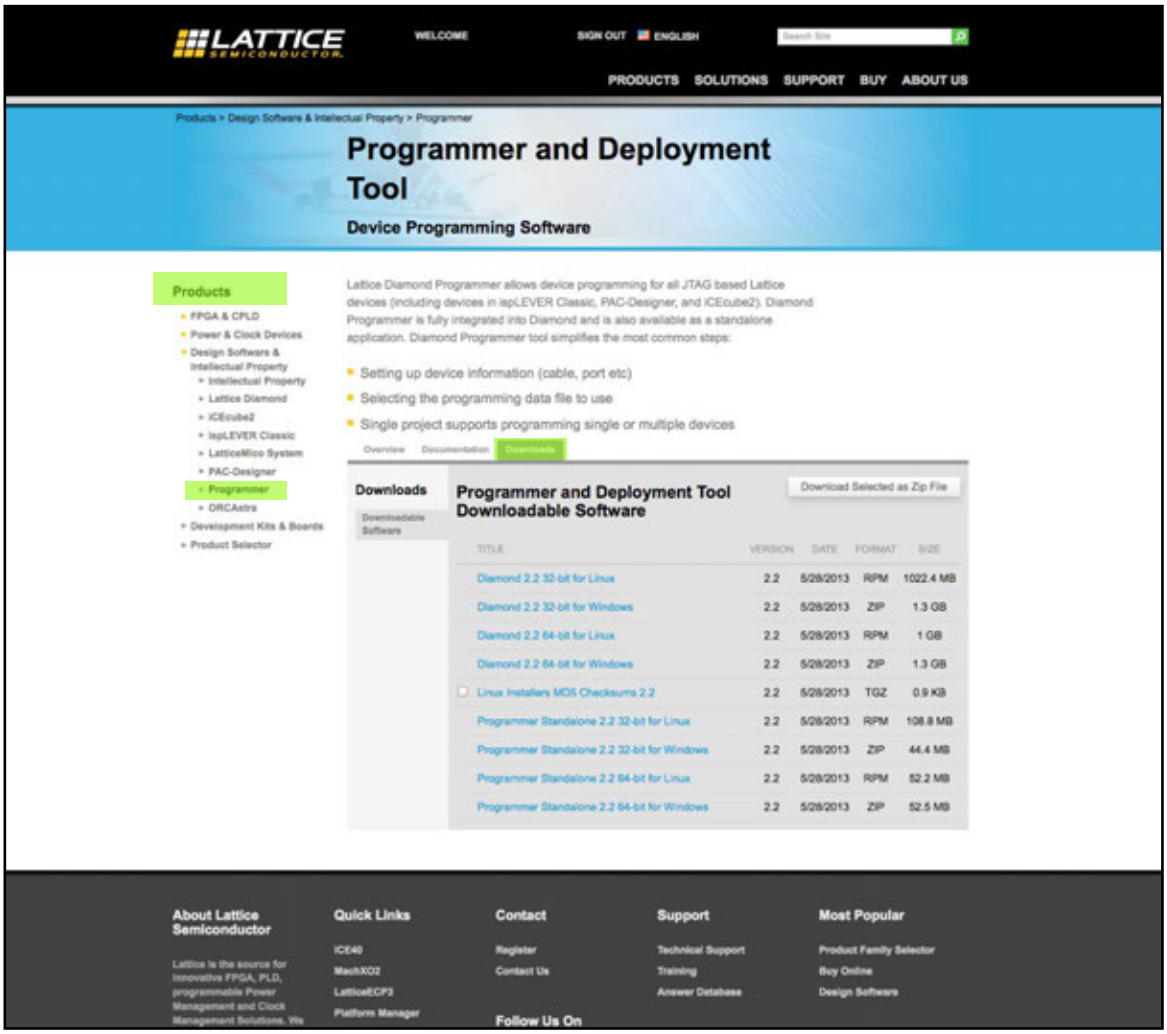
Quick Setup Guide

2.2 Downloading the Lattice Programmer



Picture 2.4: Latticesemi.com programmer download directory

Programming the LatticeECP3 device requires Lattice "Programmer Standalone". The software can be downloaded after a free registration from the Lattice web site at www.latticesemi.com

Download the "Programmer Standalone" version which fits to your operating system.
To install the Programmer, just double-click on the downloaded executable file and follow the instructions.

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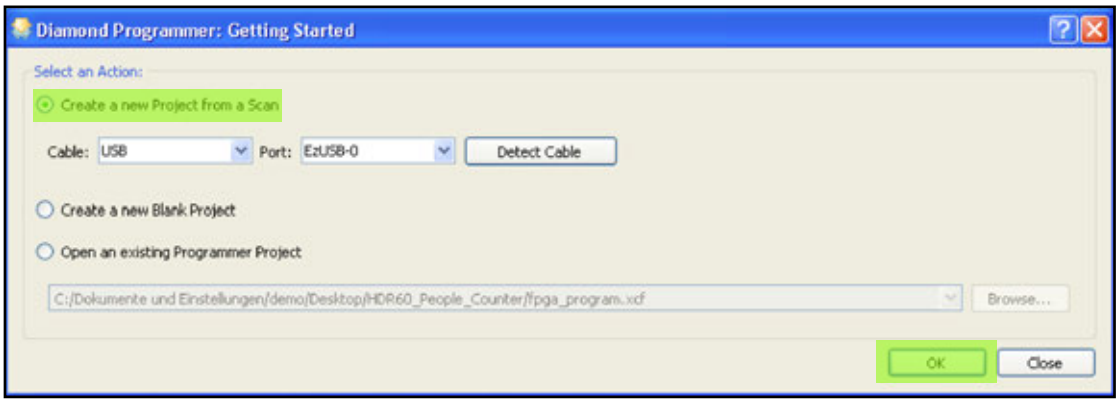
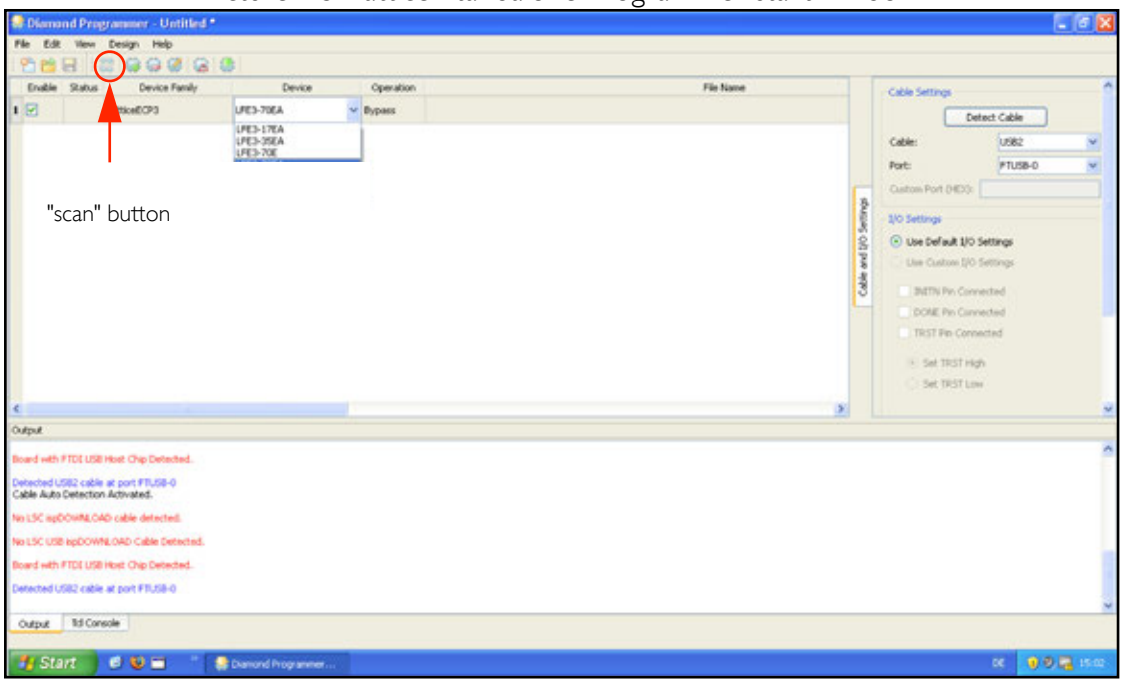
Quick Setup Guide

2.3 Programming the Bitstream

Connect the HDR60 board to its power supply, to your computer's USB and your monitor's HDMI input. Please use the upper USB Port at the HDR-60 Board. Open the programmer, select "**Create a new Project from a Scan**" and click "**OK**".



Picture 2.5: Lattice Standalone Programmer start window

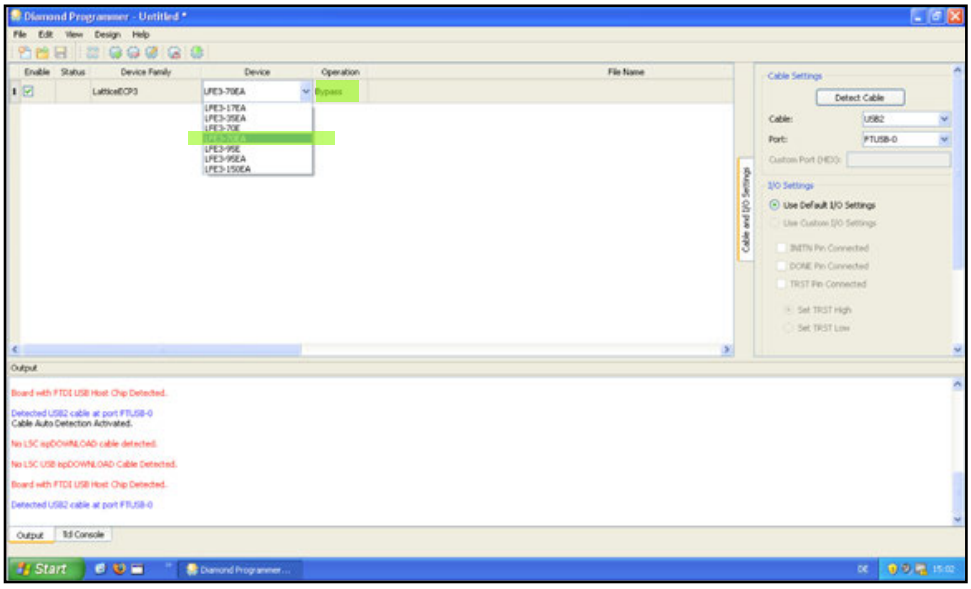


Picture 2.6: Lattice Standalone Programmer Main Window

In the next window press the button "**scan**" to find the Lattice **LFE3-70EA** FPGA.
If the scan fails, unplug the USB connector from the HDR-60 board and connect it again.
Then press the "**scan**" button. See Chapter 2.3, if the **LFE3-70EA** FPGA device is not founded automatically.

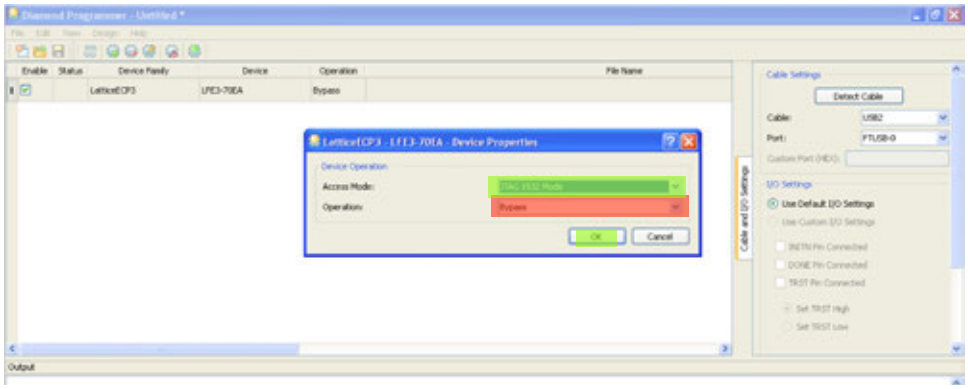
CHAPTER 2
Quick Setup Guide

2.3 Programming the Bitstream



Picture 2.7: Lattice Standalone Programmer Device Selection

If the FPGA device is not being recognized automatically, select **LFE3-70EA** from the menu manually. Next, double-click below the field "**Operation**".

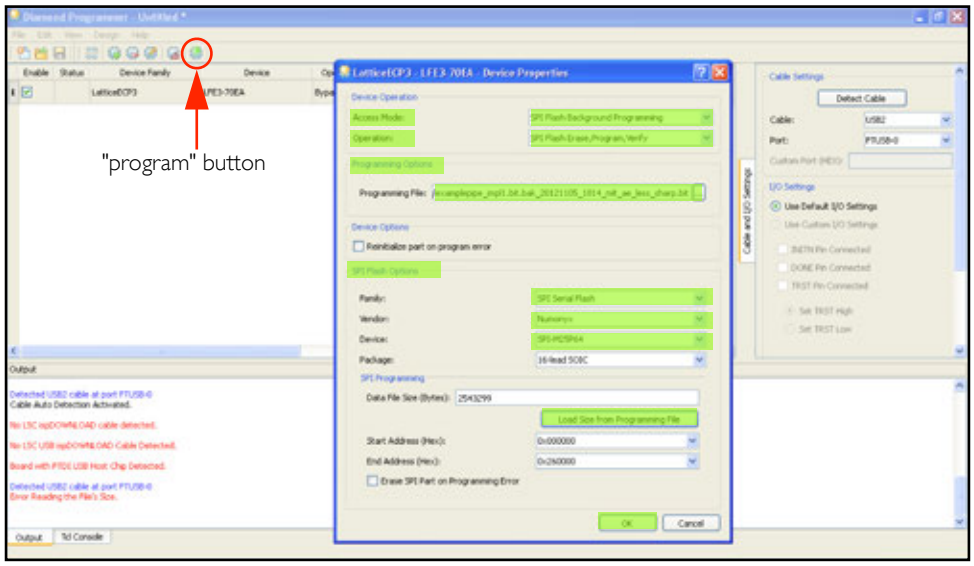


Picture 2.8: Lattice Standalone Programmer Operation Settings - JTAG Mode

Select the Access Mode "**SPI Flash Background Programming**". Set the Operation to "**SPI Flash Erase, Program, Verify**".

CHAPTER 2
Quick Setup Guide

2.3 Programming the Bitstream



Picture 2.9: Lattice Standalone Programmer Operation Settings - SPI-Flash Mode

In "**Programming Options**" set the Programming File to the bitstream* file you have downloaded from the Helionvision website. In "**SPI Flash Options**" set the Vendor to "**Numonyx**", the Device to "**SPI-M25P64**" and press the button "**Load Size from Programming File**", then press "**OK**".

Press the "**program**" button now and wait until the operation is done. This will take almost 2 Minutes.

Note:
To make the FPGA use the new bitstream, disconnect the power connector of the HDR-60 Board and connect it again.

bitstream*
Please read the instructions on page 3

CHAPTER 2
Quick Setup Guide

2.4 Starting IONOS CONFIGURATION GUI (ICG)

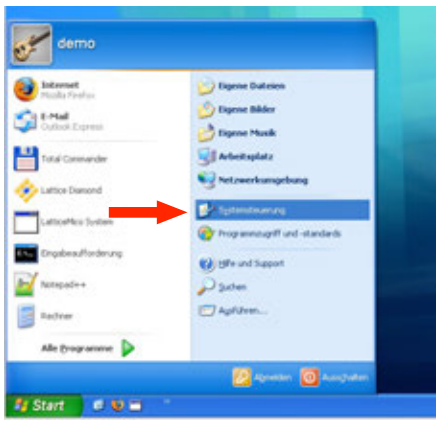
Double-click on the downloaded "**ICG installer executable**" (ICG v038....32.msi) and follow the instructions. If the ICG installation was successful you can now start ICG with the newly created **icon** on your Desktop or via the **Windows start menu**.

The ICG may ask you to reconnect the USB connection of the HDR60 board, this is necessary to start the virtual serial port which ICG uses for communication with the board.

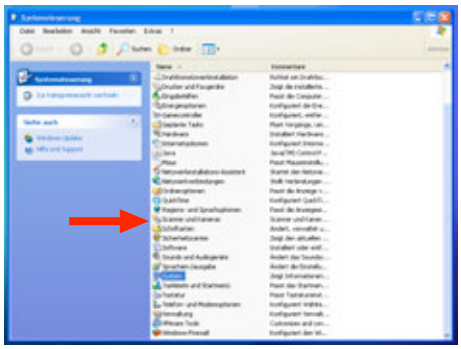
If the ICG won't start, please open the software as **admin**. If you are not allowed to use your computer as admin, please see the manual below.

2.5 Windows (XP / VISTA / 7): Activating the VCP (=virtual COM port).

Go to Start->Control Panel



Tip: If there is no entry "System" in the control panel, switch to classic view.



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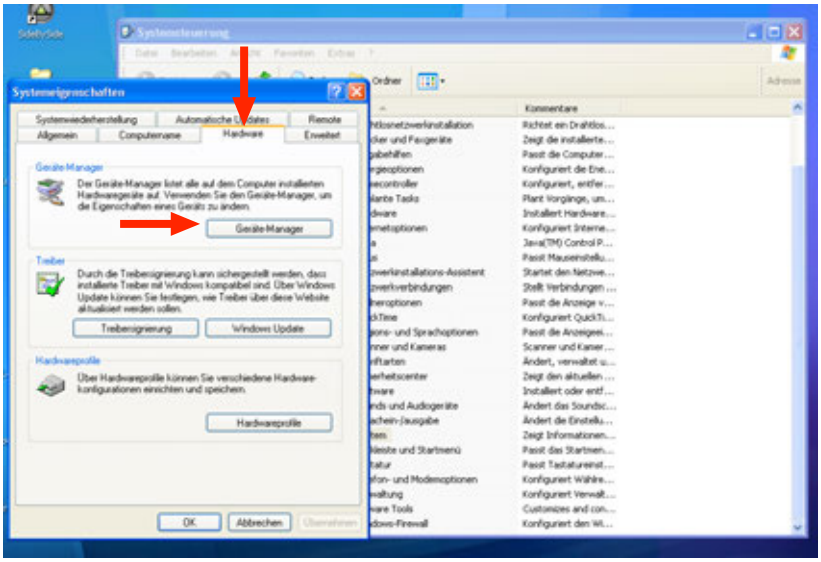
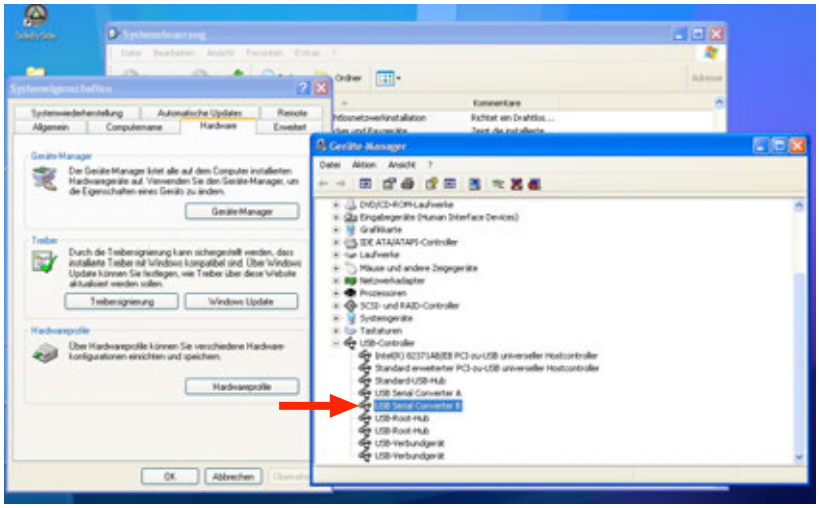
2.4 Win XP / VISTA / 7 installation instructions:

Double-click on "System" and select the Tab "Hardware"



Open the "Hardware Manager" and Double-click on "Serial Converter B".



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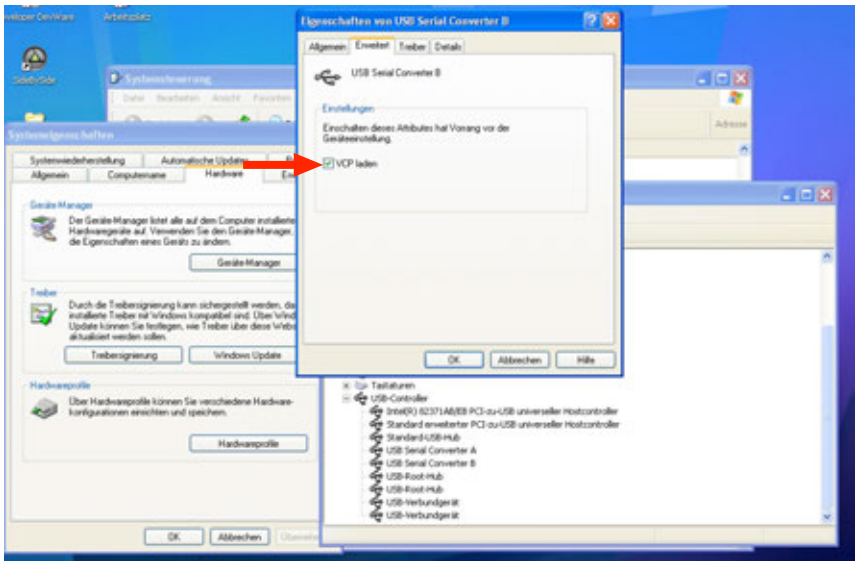
2.5 Win XP / VISTA / 7 installation instructions:

Now activate the VCP with the checkbox.



It is necessary to unplug and replug the USB cable of the HDR-60 Board.
Sometimes it might be necessary to reboot your computer.

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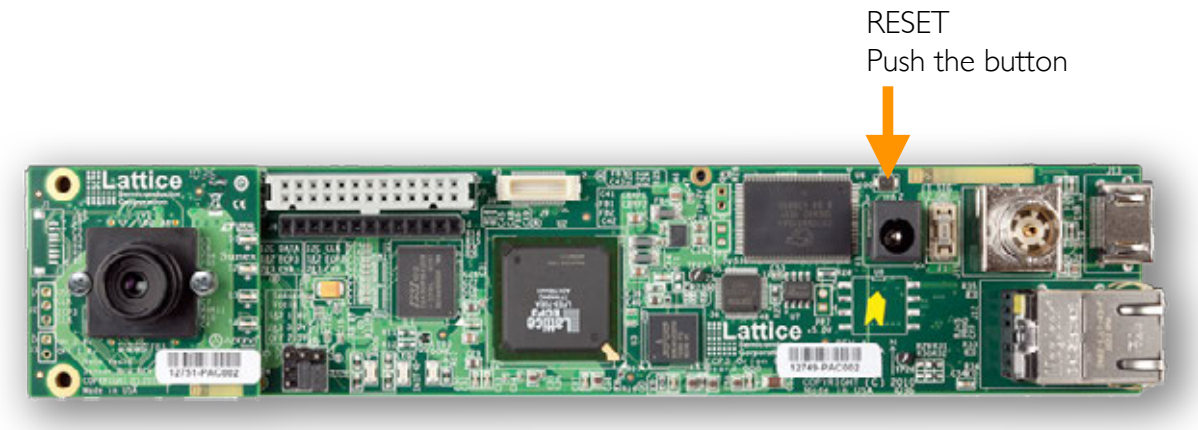
Quick Setup Guide

2.6 Hardware Button

The HDR60 board's reset button is located next to the power connector. If any problem occurs with the settings of the board, pressing this button will reset all settings to the values stored in the Flash memory.

You can also disconnect the power connector of the HDR-60 Board and connect it again.

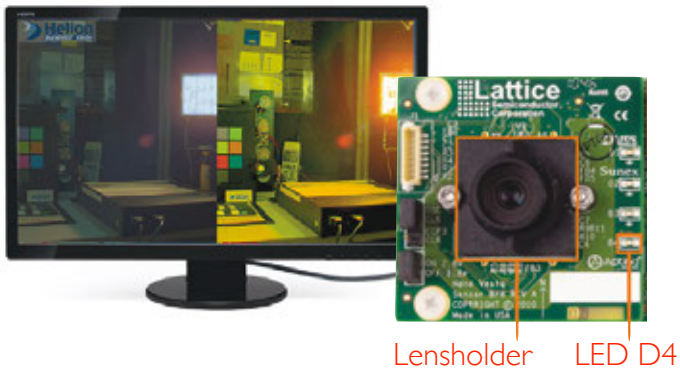


CHAPTER 3
Run the Demonstration / Kit Content

1.
Connect the NanoVesta Head Board to the HDR-60 Base Board if it is not already connected.
The two connectors permit mating only in one orientation, so no misconnection is possible.

2.
Connect the external power supply to the power connector on the HDR-60 Base Board.

3.
Connect one end of the HDMI cable to the HDMI connector on the HDR-60 Base Board and the other end to a digital monitor. It is not necessary to use the HDMI-to-DVI adapter if the display accepts also HDMI. If the display has a DVI connector, use the HDMI-to-DVI adapter. The LatticeECP3-70 device's Flash is preprogrammed to load a default demo that will appear on the monitor. Running the preloaded demonstration does not require connecting the provided USB cables to a PC.



After the AC adapter is plugged in and the HDMI cable is connected, the HDR-60 Base Board loads the LatticeECP3 with the preconfigured demo file. LED D4 will blink, indicating that the device has loaded correctly. The preloaded demo file in the LatticeECP3 incorporates an Image Signal Processing (ISP) pipeline with HDR and displays a split screen on the monitor. On your right side as you look at the monitor is the effect of the ISP pipeline and on your left side is the unprocessed image. You may need to rotate the lens holder for better focus. Here are some actions you can perform to see the ISP pipeline's capabilities:

- Auto Exposure – Cover the lens with your finger and then uncover it quickly. The picture will instantly appear with no settling time, bloom or washout. This demonstrates fast auto exposure.

- HDR – Point the lens to a light source. Note that while the light source is visible, the rest of the image is not blacked out. See the difference between the processed and unprocessed images on the split screen.

- Auto White Balance – Cover the lens for 5 seconds or more. Remove your finger and see that the Image is tinted. Wait a few seconds while the ISP reads the histograms generated by its internal Statistics block and automatically adjusts the image to natural colors. This demonstrates high-quality Auto white balance.

Note: The Demobitstream will work only 3 hours continuously. After 3 hours, you will get a black image. In this case, please turn off the external power supply for 3 seconds. After, reconnect the external power supply to the power connector on the HDR-60 Base Board. The ISP will work again for 3 hours.

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CHAPTER 4
IP-Licensing Options / Evaluation License

Procedure of SDK Evaluation (SDK = Test Drive) and Sample Source Code

Step 1
Trial (free of charge)

Kit is pre-loaded with demo bitstream
Customer can use the GUI (ICG) to setup AE, AWB, colors, contrast, gamma...

Step 2
In-depth evaluation (free of charge)

Customer has to sign free of charge **IONOS Evaluation License** by Lattice.
See also: Signing the evaluation IP licensing agreement with Lattice*
This License grants access to SW reference designs.
Customer can start first tests and developments (based on HDR-60).

Step 3
Preparation of product development and during development

Customer can buy prepaid support packages by Helion.
Support packages 01: Project Workshops
Support packages 02: Trainings (Sensor, ISP or FPGA)
Support packages 03: Consulting and Development
(Please contact: **sales@helionvision.com** for further information regarding the support packages)

Step 4
Production license and additional Project-or Site License for specific IPs (if Lattice License Model is not preferred)

Customer can sign **piece based** license agreement by Lattice
or
Project site license by Helion.

Signing the evaluation IP licensing agreement with Lattice *

Please send a mail to: sales@helionvision.com
Subject: Evaluation License HDR-60 - IONOS-ISP
Helion will forward your request to Lattice Semiconductors.

•Evaluation IP licensing:
By signing the evaluation IP licensing agreement with Lattice, customers will have access to Helion's complete IP suite at no cost. The IP suite includes documentation, **time-limited** IP cores and ISP pipeline example projects.

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CHAPTER 5
Revision History

Table 2.1: Revision History ICG Quick Start Guide

Date	Version	Section	Change Summary
2012-04-30	V01s01	-	Initial Release
2013-08-08	V01s02	-	Update of links, correction of typos
2013-09-20	V01s03	-	Update of Bitstream programming, Numbering of Images
2014-02-20	v01s04	-	License Updates